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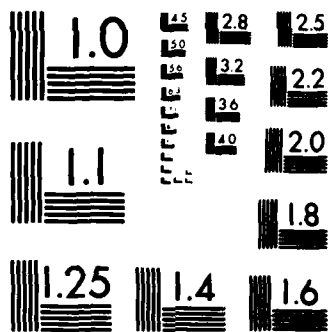
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RADC-TR-85-29
In-House Report
February 1985

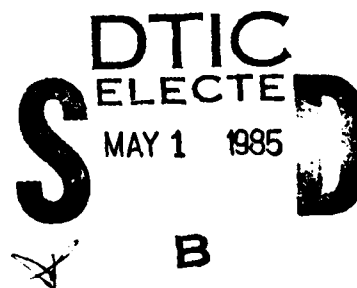


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RANDOM ACCESS MEMORY TECHNOLOGIES

Kevin W. Devaney, 1Lt, USAF

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SECURITY CLASSIFICATION OF THIS PAGE -

REPORT DOCUMENTATION PAGE

1a. REPORT SECURITY CLASSIFICATION UNCLASSIFIED			1b. RESTRICTIVE MARKINGS N/A										
2a. SECURITY CLASSIFICATION AUTHORITY N/A			3. DISTRIBUTION/AVAILABILITY OF REPORT Approved for public release; distribution unlimited										
2b. DECLASSIFICATION/DOWNGRADING SCHEDULE N/A													
4. PERFORMING ORGANIZATION REPORT NUMBER(S) N/A			5. MONITORING ORGANIZATION REPORT NUMBER(S) RADC-TR-85-29										
6a. NAME OF PERFORMING ORGANIZATION Rome Air Development Center		6b. OFFICE SYMBOL (If applicable) IRAP		7a. NAME OF MONITORING ORGANIZATION Same									
6c. ADDRESS (City, State and ZIP Code) Griffiss AFB NY 13441-5700			7b. ADDRESS (City, State and ZIP Code)										
8a. NAME OF FUNDING/SPONSORING ORGANIZATION Same		8b. OFFICE SYMBOL (If applicable)		9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER N/A									
9a. ADDRESS (City, State and ZIP Code)			10. SOURCE OF FUNDING NOS.										
			<table border="1"> <tr> <th>PROGRAM ELEMENT NO.</th> <th>PROJECT NO.</th> <th>TASK NO.</th> <th>WORK UNIT NO.</th> </tr> <tr> <td>62702F</td> <td>4594</td> <td>15</td> <td>A7</td> </tr> </table>			PROGRAM ELEMENT NO.	PROJECT NO.	TASK NO.	WORK UNIT NO.	62702F	4594	15	A7
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62702F	4594	15	A7										
11. TITLE (Include Security Classification) RANDOM ACCESS MEMORY TECHNOLOGIES													
12. PERSONAL AUTHOR(S) Kevin W. Devaney, 1Lt, USAF													
13a. TYPE OF REPORT In-House		13b. TIME COVERED FROM Feb 84 TO Jul 84		14. DATE OF REPORT (Yr., Mo., Day) February 1985									
15. PAGE COUNT 48													
16. SUPPLEMENTARY NOTATION N/A													
17. COSATI CODES			18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number)										
FIELD	GROUP	SUB GR.	Computer Random Access Memories, Silicon Controlled Rectifiers, cache memory system, Memory Chips, MOS Metal Oxide Semiconductor.										
14	03												
09	05												
19. ABSTRACT (Continue on reverse if necessary and identify by block number) <p>This report is the result on an in-house study of random access memory technologies. In addition to silicon, other technologies are investigated, such as gallium arsenide, silicon-on-sapphire, silicon-on-insulator, and magnetic bubble.</p>													
20. DISTRIBUTION/AVAILABILITY OF ABSTRACT UNCLASSIFIED/UNLIMITED <input checked="" type="checkbox"/> SAME AS RPT. <input type="checkbox"/> DTIC USERS <input type="checkbox"/>			21. ABSTRACT SECURITY CLASSIFICATION										
22a. NAME OF RESPONSIBLE INDIVIDUAL Kevin W. Devaney, 1Lt, USAF			22b. TELEPHONE NUMBER (Include Area Code) (315) 330-4581		22c. OFFICE SYMBOL RADC (IRAP)								

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SECURITY CLASSIFICATION OF THIS PAGE

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GLOSSARY OF TERMS

- Bipolar:** A transistor which conducts by means of both holes and electrons.
- Dynamic RAM:** A memory which requires repetitive refreshing operations in order to retain stored information.
- Functional Throughput Rate:** The figure of merit applied to VHSIC chips. It is computed by the product of the on chip clocking speed (the reciprocal of 4 gate delays) in Hertz and the gate density in gates/cm.
- MESFET:** Metal-semiconductor field effect transistor.
- MOSFET:** Metal-oxide semiconductor field effect transistor.
- Pseudostatic RAM:** A dynamic RAM which internally generate its own refresh operations.
- Rad:** The radiation dose that causes an energy absorption of 200 ergs. It is relative to the absorbing material. However, on rad (silicon) only differs about 6% from on rad (gallium arsenide).
- Soft error:** The loss of information in a dynamic RAM memory cell due to radiation.
- Static RAM:** A memory which does not require repetitive refresh operations to retain stored information.

INTRODUCTION:

This paper is the result of an in-house study of random access memory technologies. Silicon, of course, has a firm grip on the computer industry, and the different silicon processes are discussed. However, many alternative technologies are under development. Gallium arsenide and Josephson junctions have been pursued in hopes of higher speeds and lower power consumption. Silicon on sapphire and silicon on insulator have been developed to enhance silicon's performance and eliminate such problems as latch up. Finally, the need for data retention when power is lost has spawned the existence of non-volatile memories, not only in silicon, but also in magnetic memories. Each technology's strong points and drawbacks are presented, as well as the hurdles to be overcome for further development. Emphasis is given to requirements for military applications, such as a wide temperature range and radiation hardness. In this light, it is fitting that the Department of Defense's VHSIC program and its Phase I memories are also described in this paper.

Operator-supplied key words included: - P. 1422

MEMORIES:

As a computer operates, the instructions and data being processed are constantly being taken out of and put into its memory. The stored-program concept, and the power of computer programming are derived from the memory's ability to access randomly; to place a word into any address and to subsequently fetch it. Random access is contrasted with serial access, where information must be stored and retrieved in definite sequences, and it is usually necessary to wait for irrelevant material to flow by in order to retrieve the desired information. In order to distinguish them from read only memories (ROMs), random access memories (RAMs) are also referred to as read/write memories. The most significant benefit of random access memory is the ability to choose one or another operation depending on the outcome of the process being executed, thus permitting conditional branching and looping.¹

Besides the main computer memory which holds stored programs and data, random access memories (RAMs) have other applications. A scratch pad memory is a small, fast memory used for temporary storage of interim calculation results from the central processor of the computer. A buffer memory is another small, fast memory which is used to hold data for transfer between sections of a computer, between a mainframe and peripheral equipment, or between separate units of a large system.²

A cache memory is a small, fast memory which holds that portion of the main memory that is currently being used. Since most micro-processors process instructions sequentially, it is possible to reduce the cycle time by keeping the instructions in the cache memory with its faster access time. This technique is effective as long as the "miss rate" is much less

than the ratio of the cache access time to the main memory access time. The miss rate is the fraction of times the cache memory does not hold the needed instruction or data, due to branching or a discontinuity in the program. The introduction of the cache memory system was an improvement in the cost/performance ratio of computer memory systems. 3

SILICON MEMORIES

Memory technology has come a long way from the vacuum tubes and mercury delay lines of the 40's and 50's. Silicon semiconductor memories first appeared on the IBM System/360 Model 85 in 1969, and replaced magnetic core for main memory applications around 1977 when the availability of 4K and 16K chips made silicon cheaper per bit. The unrelenting push for denser, higher capacity RAMS continues to drive the semiconductor industry at a breakneck pace. Already, laboratory versions of the 1 megabit RAM are appearing.

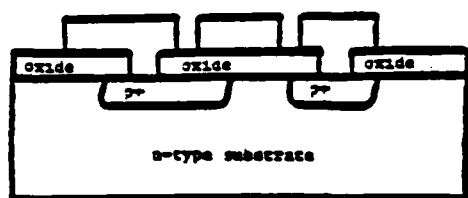
There are two basic types of RAMs: static and dynamic. Dynamic RAMs allow higher densities than their static counterparts, because each memory cell requires only one transistor rather than four or six. Dynamic RAMs also consume less power than static RAMs of the same capacity. The information in a dynamic RAM memory cell is stored as a voltage on a capacitor, and the transistor acts as a switch. Because the charge leaks off the capacitor, the dynamic RAM must be refreshed every few milliseconds. Also, since reading out the data requires discharge of the capacitor, internal circuitry must rewrite data into the memory each time it is read.

Static RAMs use bistable flip-flops to store information. They require no refresh, and typically offer faster access times than dynamic RAMs. In the flip-flop, one transistor is always on, and this accounts for the static RAM's higher power consumption. Static RAMs are also more expensive than dynamic RAMs, and this fact has spurred the development of the pseudostatic RAM. The pseudostatic RAM is a dynamic RAM which internally generates its own refresh cycles, and thus acts like a static

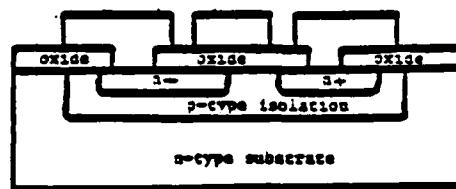
RAM. Its cost, performance, and power consumption are a compromise between those of static and dynamic RAMs.

The first silicon technology was bipolar, which began development in 1960, and was applied to memory fabrication in 1963. Bipolar technologies, such as emitter-coupled logic (ECL), have an advantage in speed of about a factor of five over competing metal oxide semiconductor (MOS) technologies. However, because of problems with high power dissipation and defect sensitivities, bipolar integration is about an order of magnitude behind MOS. Because of this fact, bipolar memory chips are largely limited to 16K capacities and below, for scratch pad, buffer, and cache memory applications. The state-of-the-art in bipolar memory is Fairchild's 16K static RAM which has an access time of 25 nanoseconds and consumes 705 milliwatts.

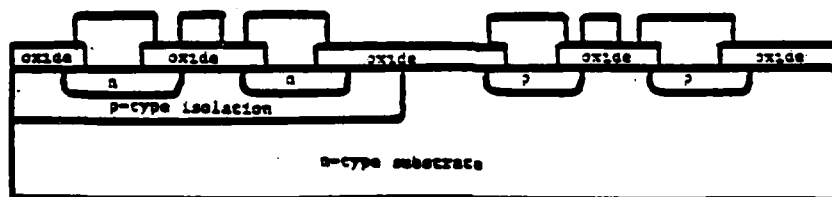
Metal oxide semiconductor (MOS) technologies dominate large capacity, high density applications. Most early development was done with p-channel MOS, and the first commercially acceptable PMOS memory was Intel's 1K RAM which was introduced in 1970. N-Channel MOS was initially the more difficult technology, but offered higher performance potential, and quickly became dominant. IBM put the first 1K NMOS memory into production in 1971. Complementary MOS technology uses matched pairs of n- and p-channel transistors. CMOS was invented in 1962, but was restricted to low power applications (calculators and watches) and was not developed for high speed, high density devices until very recently. The different silicon MOS technologies are shown in Figure 1.



p-channel MOS transistor



n-channel MOS transistor



complementary MOS transistors

FIGURE 1. SILICON METAL OXIDE SEMICONDUCTOR (MOS) TECHNOLOGIES

For many years, NMOS was the industry leader for high density memories, and this is reflected by the fact that all of the 256K RAMs in production this year are NMOS devices. However, CMOS is rapidly replacing NMOS as the technology of choice, and is expected to capture nearly half of the entire integrated circuit market by 1990. The laboratory versions of the 1 megabit RAM all use CMOS, and improvements are being made from the 256K level down with CMOS technology.

A major reason for the shift to CMOS is the need to reduce power dissipation and chip operating temperatures. Current packaging technology limits total chip power dissipation to about 1 watt in order to avoid high temperatures that cause reliability problems, such as electromigration. NMOS was originally a "ratioed" circuit technique, where the choice of

transistor widths and lengths exist in a delicate balance. This type of logic has the inherent problems of high power dissipation and low noise immunity. In the late 1970's the move from 5 μm to 3 μm design rules increased chip densities and power dissipation. As a result, NMOS technology switched to "ratioless" logic and NMOS designs began to look like CMOS designs. CMOS circuits had always been "ratioless" since their invention. Despite NMOS' switch, CMOS still retains an edge in power dissipation and noise immunity.

CMOS also has an advantage over NMOS in immunity to soft errors, which are a problem in high density dynamic RAMs. Soft errors are caused by alpha particles generated from cosmic rays or contaminants (such as uranium or thorium) present in the device packaging material. An alpha particle can penetrate about 10 microns into silicon, and produce enough current to discharge the capacitor which is the basic memory element in a dynamic RAM. Certain CMOS designs have been found to reduce this problem significantly.

CMOS has always been plagued by a problem known as "latch-up." Neighboring p- and n-transistors tend to act like silicon-controlled rectifiers (See Figure 2). When input and output voltages wander outside recommended limits, these SCR's turn on and draw excessive current. Several techniques have been used to avoid "latch-up", such as reverse-biasing, greater horizontal spacing, guard bands, and metal straps to critical areas. However, at higher densities, latch-up will prove more difficult to overcome.

SILICON ON SAPPHIRE

Silicon-on-sapphire (SOS) structures are used mostly with CMOS technology. The use of an insulating substrate such as sapphire (also called aluminum oxide, Al_2O_3) offers several advantages over bulk silicon devices. Leakage currents and parasitic capacitances between adjacent devices, between devices and the substrate, and between interconnections and the substrate, are virtually eliminated. Since switching speed is directly proportional to capacitive load, SOS devices are faster than their bulk silicon counterparts. Also, because parasitic pnpn devices are eliminated, latch-up problems are avoided, and CMOS/SOS structures can be made 30% smaller than their bulk CMOS counterparts. This results in improvements in density, reduction of power dissipation, as well as further increases in switching speeds.

Another advantage of SOS technology is radiation hardness. Commercial devices can usually withstand radiation doses of around 10^4 rads; however, airborne and spaceborne applications may require immunity to doses of up to 10^6 rads or more. Because CMOS/SOS devices provide a minimum p-n junction area, radiation-induced junction currents are reduced, making these chips radiation hard. Most rad-hard CMOS/SOS chips can withstand a total dose of 10^6 rads, but memories have not been able to achieve this level of immunity. Problems with radiation induced leakage currents at the edge of the silicon-on-sapphire island have limited RAM hardness to 10^5 rads. The first 4K static RAMs appeared in 1982, with a 300 ns access time and operable throughout the military temperature range. In 1985, a 16K static RAM will be available with the ability to withstand a total dose of 4×10^5 rads. Its projected access time is 70 nanoseconds. Also,

The WAM will be used to perform basic recognition functions. Upper and lower limits of six fields in a 48-bit input word are stored in the WAM in eight sets. An input word is then simultaneously compared against the limits of each stored word. Several options exist depending whether the word was recognized or not.

Several innovations will be necessary to make Phase 2 a success. Work is being done on x-ray and e-beam lithography to provide the resolution required for .5 um geometries. However, this is not the limit to the technology, according to the Department of Defense. Another program, known as USER (Ultrasmall Electronics Research), is geared toward the 10-20 nanometer range. Radically new electronic device structures will have to be invented to operate under the physical properties which govern this regime.

dose of at least 10^{11} neutrons/cm². These chips must also be highly reliable, having failure rates of not more than .006% per 1,000 hours after screening and burn-in. VHSIC also calls for computer aided design techniques to minimize customization and provide for ease of testability.

Out of the 28 VHSIC Phase 1 chips, five are memories. One of the five is Westinghouse's 64K static RAM with a 20 ns access time. The chip will be fabricated with CMOS technology. Texas Instruments is using NMOS technology to produce a 72K static RAM that accesses in 35 ns. This chip also has special features like on chip parity and error correction, and programmable write protection, to protect against accidental writes.

TRW is being contracted to produce three innovative memories for VHSIC Phase 1. One of these is the 4K 4-port memory. The memory shall have two write ports and two read ports, all of which can be utilized independently and simultaneously, with access to the entire memory array. This device accesses in 40 ns, and is expected to lead to larger capacity 4-port memories. In addition, the memory will be able to handle situations of contention, such as two simultaneous writes to the same location, or a simultaneous read and write to the same location.

The other two are associative memories: the content addressable memory (CAM) and window addressable memory (WAM). The CAM will be organized as 32 words of 48 bits each. During operation a 48 bit word will be inputted, and the chip will output an address indicating which register's contents, if any, exactly matches the input word. If no match occurs, the chip will signal this result. If more than one match occurs, a prioritized polling procedure helps cycle through the addresses.

have nearly closed the IC technology gap. It is this development which gave birth to the Department of Defense's VHSIC program.

The VHSIC program's goal is to increase the processing speeds of military microchips by a factor of nearly 100. The program also calls for improved radiation hardness, reliability, and testability. Consideration will be given to minimizing acquisition costs as well as to maximizing ease of insertion of VHSIC technology into systems.

VHSIC stands for Very High Speed Integrated Circuits, and is divided into four phases. Phase 0 began in March 1980 to provide a plan and approach for Phase 1 and Phase 2. (\$12.3M). Phase 1 calls for 1.25 um design rules, and a functional throughput rate (FTR) of 5×10^{11} Gate Hz/CM². This is a threefold improvement over present throughput rates. Phase 1 began in May 1981 with six prime contractors and funding of \$167.8 million.

Phase 2 of VHSIC will require .5 um design rules, and FTR of 10^{13} Gate Hz/CM². Total funding is expected to be \$83.6 million. Phase 3 began in 1980 and runs concurrently with the other phases of the program. This effort consists of 59 contracts for a total of \$35.8 million to industry and universities for solution of various technical problems in Phase 1 and Phase 2. Work is also being done outside the various phases in areas such as technology insertion and yield enhancement, bringing total VHSIC program cost to \$680.1 million.

All VHSIC chips must operate throughout the full military temperature range (-55°C to +125°C). Also, they must be capable of operation in a radiation environment of 10^4 rads without upset. They must be able to withstand a transient radiation dose of 10^8 rads/s, and neutron radiation

MILITARY MEMORIES

Microchips used for military applications are subjected to more stringent requirements than those used in the commercial sector. Military standards for microcircuits are contained in MIL-M-38510, General Specification for Microcircuits, and MIL-STD-883, Test Methods and Procedures for Microelectronics. The military requires the chips to be highly reliable, and capable of operation over a wider temperature range (-55°C to +125°C as compared to 0° to 70°). Also, radar and signal processing applications require faster devices than are normally needed in commercial systems. As a result, these application-specific chips must be custom designed and fabricated, making them more expensive, and causing their development to lag three or more years behind the commercial sector.

Memory chip capacity for military applications is limited to 16K, with typical access times of 50 ns. So far, manufacturers have not been able to produce 64K RAMs which operate throughout the full military temperature range, although they are expected to be available by the end of the year. To compensate for this, manufacturers have resorted to a modular approach, mounting several or more 16K chips onto one package, achieving capacities of up to 512K.

The military integrated circuit development lag is due to DoD's ever-diminishing share of the market. The military's portion of the microelectronic market decreased from 70% in 1965 to about 7% by 1980. Therefore, while the VLSI revolution is underway, its fruits are not being directed toward defense applications. In the Soviet Union, the integrated circuit market is dominated by the military, and as a result the Russians

However, there are problems with mask distortion when beam heating occurs, as well as scattering effects. Also, it is much more difficult to focus the ion beam than the electron beam.

An unexpected obstacle to even higher circuit density is the interconnection problem. Speed and performance are now limited by the resistance-capacitance (RC) time constants of the interconnections between active components. Metal silicides are now being used to replace at least one layer of polychrystalline silicon interconnections because of their lower resistivity (two orders of magnitude lower). Work is also being done to increase the number of interconnection levels, allowing individual lines to be shorter, thereby lowering both R and C. Another problem is that interconnections have become the limiting factor to chip density, rather than the area taken up by active components such as transistors. Many experts feel that it is useless to develop gallium arsenide in pursuit of higher speeds unless a breakthrough is made with respect to interconnection techniques.

(.35 μm), at the expense of higher cost and lower wafer throughputs. However, even with smaller wavelength ultraviolet light (2500 \AA), diffraction effects will limit optical lithography resolution to between .5 μm and 1 μm .

Several techniques under development to satisfy future resolution requirements are electron beam, ion beam, and x-ray lithography. Electron beam lithography is not limited by diffraction effects (the deBroglie wavelength of the electrons is about 1 \AA), but by the diameter of the electron beam. As a result, high resolution (.1 μm) and precise alignment (.1 μm) can be achieved. No masks are required, eliminating mask-related defects, and improving yields. A computer drives the e- beam to write all the necessary patterns directly onto the resist-covered wafer. One drawback to this method is the low wafer throughput which makes it expensive. Work is being done on multiple beam projection and beam shaping techniques to make e-beam lithography more cost effective. Also, extremely thin photoresist layers must be used to minimize electron backscattering effects.

X-ray lithography also has been able to provide high resolution (< .5 μm) because of its small wavelength (10 - 50 \AA). X-ray has a higher wafer throughput than e-beam, although its speed is somewhat hampered by weak radiation sources and slow resists. Also, there have been problems in the construction of masks, which consist of an x-ray transmissive membrane with a window pattern created by a metal absorber.

Ion beam lithography is an offshoot of x-ray lithography, where 200 keV protons have been substituted for the x-rays. An improvement in wafer throughput can be made because of better resist sensitivity to protons.

Current mass production techniques use 2 μm design rules. The laboratory versions of the 1 Mbit chip have gotten down to the .8 μm level. Phase I of the VHSIC program, nearing completion, calls for 1.25 μm design rules, while Phase II will require .5 μm devices. Most experts feel the fundamental limits of device scaling will be reached somewhere between .25 μm and .5 μm . One reason is that the breakdown voltage for MOS transistors will continue to decrease with device scaling. The supply voltage must be lowered from 5V to 3V in order to get down below .7 μm geometries. Another problem is that continued scaling of the gate oxide down below 50 \AA will introduce tunneling effects, and defect densities may also cause problems. Also, as the devices inside the chip get smaller, the number of dopant atoms in each region also decreases, and statistical fluctuations become significant. These fluctuations will cause troublesome variations in the threshold voltages of the devices. Problems of high current densities, hot electrons, and ionizing radiation will also prove to be limiting factors for semiconductor device scaling.

A fundamental part of the microchip manufacturing process is optical lithography. A radiation-sensitive emulsion called photoresist is deposited onto the silicon wafer, and a pattern is exposed onto the wafer through a mask with ultraviolet light. The exposed (or unexposed) areas are then chemically dissolved or "etched". Then any substrate doping or oxidation is accomplished, and the process is repeated, using anywhere from 7 to 14 masks depending on the complexity of the chip. Several optical lithography techniques employed are contact, proximity, 1:1 projection, and step-and-repeat. The step-and-repeat process has brought about improvements in resolution (1.3 μm) and alignment

Moore's law for silicon (originated by Gordon E. Moore of Intel), held that the scale of integration doubles every year. Around the late 70's, this progress slowed to a quadrupling of chip densities every three years. Each fourfold increase in memory chip capacity has been achieved through a doubling of packing density, 1.4 times greater design cleverness, and 1.4 times greater chip size. Packing density is increased through device scaling. This refers to reduction of the physical dimensions of the transistor, resulting in increased speeds, and lower power dissipation, in addition to higher packing densities. In order to keep the electric field the same inside the device (thereby avoiding undesirable high-field effects such as mobility degradation, impact ionization, and hot electron injection), and maintain the same 5V supply voltage (for systems compatibility), the doping concentration of the silicon must be increased proportionately. The effects of scaling are listed in Table 2.

Device Dimension	1/K
(lengths and widths of conductors and transistors, depths of junctions, and thickness of the gate oxide)	
Doping Concentration	K
Voltage	1
Propagation Delay	1/K
Power Dissipation	K

TABLE 2. EFFECTS OF SCALING

A testability problem has arisen with the advent of redundancy to improve manufacturing yield. It is impossible to effectively test chips with redundant circuits because of the inability to detect externally whether or not a chip has been repaired. Manufacturers will have to use a "silicon-signature" method to enable testers to identify which addresses have been repaired. Siemens AG, of West Germany makes a 256K RAM which has this feature.

The most effective way to reduce production testing time and tests is to design-for-test. A deliberate effort must be made to ensure that VLSI circuits can be tested thoroughly with the least amount of time and cost. A great deal of work is being done in this area, and memories are being created with on-chip test capability. In the future, chips will be able to diagnose their own faults and redirect functions from the failed circuit through the appropriate redundant circuit.

A problem peculiar to dynamic RAMs is maintaining adequate capacitance in the memory cell as bit densities demand more miniaturization. A capacitor of 50 femtofarads is considered the minimum necessary to guard against soft errors, and maintain a sufficiently high signal-to-noise ratio. (A capacitor of 50 femtofarads charged to 5 volts holds 250 femtocoulombs, which corresponds to about 1.5 million electrons, about the minimum charge that can withstand an alpha-particle hit.) A major breakthrough in this area has been made with the introduction of the corrugated capacitor cell (CCC) by Hitachi. This capacitor uses a vertical structure, called a moat, to achieve a 60 femtofarad capacitance in a 21 um^2 memory cell. This is more than twice the performance possible with conventional capacitor structures.

which can then be cut off. Zone refining is used mostly to provide high resistivity wafers for specialized applications such as high voltage and power devices.

The Czochralski method uses a seed crystal which is partially immersed in molten refined silicon. The crystal is slowly withdrawn, and a single crystal is grown by progressive freezing at the liquid-solid interface. Both the melt and puller are continuously rotated, to produce a more homogeneous crystal. This technique provides larger diameter wafers, and produces over 80% of all silicon wafers used for integrated circuits.

The application of magnetic fields to the Czochralski method results in improved wafer purity and uniformity. This will allow growth of higher resistivity, lower defect, and larger diameter silicon wafers. This technique was developed by the Japanese in their government-industry VLSI program. Work is also being done under the DoD's VHSIC program to improve silicon quality using magnetic Czochralski technology.

Another problem which comes with increasing density and complexity is the test bottleneck. The time required to adequately test a memory chip has undergone a dramatic increase, to the point where it now takes more than five minutes to test a 256K RAM.

Test patterns of 0's and 1's have been devised to check for faults within chips. Running these patterns through many chips in parallel can reduce test times considerably. Still, some tests such as soft error and reliability testing require too much time to be executed as part of production testing. These types of failures must be controlled by engineering characterization and lot sampling.

SILICON AND THE FUTURE:

Several innovations are necessary in order to go beyond the 256K level. Redundancy was originally introduced in 64K RAMs, and is becoming increasingly important at high densities. As integrated-circuit features get smaller, defects that were formerly insignificant start to cause problems. The probability of faults has increased with larger capacity memories and smaller circuits within those memories. As a result of this development, manufacturers have introduced spare rows and columns into memory chips. This is done with a slight increase in chip size and only a minor penalty in access time. Repair is done when the chips are tested. Laser beams or fuse blowing are used to implement the redundant circuits.

Originally, some manufacturers claimed that use of redundancy was a "copout", and that chips which required the use of extra circuits were of inferior quality. These chips which had to be fixed were presumed to have a higher rate of failure than those which were fault-free, since chip manufacturing processes basically follow negative binomial statistics. However, as the technology has moved down to two micron design rules and below, redundancy has become absolutely necessary to keep manufacturing yields at acceptable levels. As a result redundancy has been implemented throughout the semiconductor industry.

Work is also being done to improve the quality of the silicon wafer used in integrated circuit production. Two techniques are used for the purification of silicon: zone-refining and the Czochralski methods. Zone refining selectively heats a long, thin ingot, moving the molten region back and forth across the rod. Impurities are more likely to stay in the molten region, and can be moved almost completely to the ends of the rod,

<u>MANUFACTURER</u>	<u>CAPACITY/TYPE</u>	<u>TECHNOLOGY</u>	<u>ACCESS TIME</u>	<u>POWER DISSIPATION</u>
MOTOROLA	256K DYNAMIC RAM	NMOS	100ns	350mw ACTIVE 20mw STDBY
INMOS	64K DYNAMIC RAM	NMOS	100ns	413mw ACTIVE 22mw STDBY
FAIRCHILD	16K STATIC RAM	BIPOLAR (ECL)	25ns	705mw TYPICAL

TABLE 1. MEMORY CHIP CAPACITIES AND PERFORMANCE

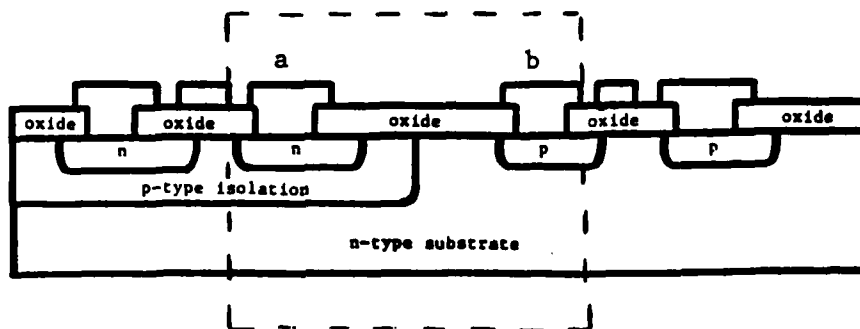


FIGURE 2(a). CMOS STRUCTURE



FIGURE 2(b). CMOS STRUCTURE SEEN AS A SILICON-CONTROLLED RECTIFIER (SCR)

The highest capacity memories in volume production are 256K RAMs with access times of around 100 ns. The current volume leader is Hitachi, which claims to be turning out 100,000 devices each month. In 1985, 256K devices should be in plentiful supply, with eight U.S. and six Japanese firms competing at this level. The performance available at each density level is given in the table below:

work is also being done on a 64K device with a 50 ns access time, and radiation immunity up to 10^6 rads.

An interesting footnote to this is the fact that similar radiation hardening has been achieved with bulk CMOS through the use of guard banding. A 4K static RAM which can withstand a total dose of 10^5 rads is available with a 200 ns access time, and can operate throughout the full military temperature range. In the laboratory, 16K devices have been fabricated which can withstand a dose of 10^6 rads without upset.

One major drawback to SOS technology is the price of the sapphire substrate, which is about seven times as costly as silicon. For this reason SOS is limited primarily to military applications. Also, a high density of defects at the silicon/sapphire interface has limited carrier mobilities to values smaller than those of bulk silicon. Carrier lifetimes are also low, preventing SOS from being used for bipolar applications and dynamic RAMs. As a result, for memory applications this technology has been used only in CMOS static RAMs. Another drawback to SOS is that its performance edge over bulk silicon will erode below 1.2 micron design rules as interconnect capacitances become more dominant.

SILICON-ON-INSULATOR

The problems and expense associated with silicon-on-sapphire have lead to the development of silicon-on-insulator (SOI) as its low-cost successor. Researchers wish to retain the advantages of an insulating substrate, such as increase speed, high density, radiation hardness, and elimination of latch-up problems without the high cost of sapphire. Also, some SOI processes permit the fabrication of three-dimensional integrated circuits, which would lead to revolutionary device structures.

Several different techniques are being used to manufacture SOI devices. One such approach is recrystallization, which starts with a polysilicon film on an insulating substrate such as silicon dioxide (SiO_2). The polysilicon is melted using a laser beam, electron beam, or graphite strip. When the silicon freezes, it will form large grains or single crystals (if a seed crystal is used). So far, these techniques have only produced test chips, although good results have been achieved. The graphic strip heater method does not permit fabrication of 3-dimensional circuits, because the high temperatures ($> 1400^\circ\text{C}$) involved would destroy any circuits already present. Laser recrystallization allows better precision in the transfer of energy, and the lower temperatures used will permit vertical integration.

Another method is Epitaxial Layer Overgrowth (ELO), which is accomplished using mature, well-developed silicon chemical vapor deposition (CVD) technology. The silicon layer is seeded in the openings of a silicon dioxide mask, and growth rates of 1 $\mu\text{m}/\text{minute}$ have been achieved. The major disadvantage of the ELO techniques is a low horizontal to vertical growth rate ratio, which has been reported as

high as 40:1, but films with low defect densities can only achieve a ratio of 1.5:1. In order to be considered as a straightforward replacement for SOS, this ratio must be increased to 50:1 without a sacrifice in quality, so that areas of 50 μm or more of insulating substrate can be covered with a .5 μm film.

Separation by implanted oxygen (SIMOX) is another SOI process. This technique implants oxygen ions about 50 to 120 nanometers below the surface of a silicon wafer to convert a .5 μm thick layer to silicon dioxide. Usually an additional .5 μm thick layer of silicon is grown on the wafer by conventional chemical vapor disposition. Latch-up free, 1K CMOS RAMs have been fabricated with a 10 ns access time. One drawback to this process is that the extremely high doses of oxygen required ($\sim 10^8/\text{cm}^2$) takes present implanters about 10^3 - 10^4 seconds per wafer. A twenty-fold increase in oxygen flow will be necessary to attain a throughput rate suitable for production.

Full isolation by porous oxide silicon (FIPOS) begins with a silicon wafer which undergoes selective p^+ layer formation, and then the upper portion is converted to n^+ by proton implantation. Next hydrofluoric acid is used to change the p^+ type silicon into porous silicon, while the n^+ type silicon is unchanged. The porous silicon is then selectively oxidized and the n^+ layer is changed back to a p^+ layer. This process has been able to achieve high quality isolated silicon layers, and a 16K CMOS static RAM has been fabricated with a 35 ns access time. The only drawback to this technology is that the steps necessary to create porous silicon are not compatible with present integrated circuit production techniques. Although this process is not applicable for three-dimensional

circuits, it seems to have the best chance of replacing silicon-on-sapphire.

Graphoepitaxy induces a crystal structure in a silicon film through the use of a pattern relief structure in the insulating substrate. This film has been formed using chemical vapor disposition or laser recrystallization, with the best results coming from the latter method. Still, there are problems with grid preparation, and the mechanisms involved in this process are not well understood.

Most experts feel that silicon-on-insulator technology is about three years from fruition. While most research is being sponsored for military applications, the commercial market will also benefit from this technology. Both static and dynamic CMOS RAMs should be available using 1 um design rules, or less. Also, SOI technology is suitable for bipolar technology, although so far it has been limited mostly to CMOS applications.

GALLIUM ARSENIDE

Gallium arsenide is a semiconductor material having a higher electron mobility than silicon, with electron velocities as fast as 5×10^7 m/s (about five times as fast as silicon). The reason for this is the shapes of the conduction bands for the two semiconductors. In addition to high speed, gallium arsenide devices offer such advantages as low power consumption, wide temperature range (-200°C to $+200^\circ\text{C}$), and superior radiation hardness (up to 5×10^7 rads). These characteristics have lead to the recent vigorous development of gallium arsenide for defense applications, as well as the next generation supercomputers.

The depletion-mode metal-semiconductor field-effect transistor (D-MESFET) is the most mature GaAs process, having been developed for ten years, and producing the first LSI (300-3000 gates) chip in 1980. Thus, it follows that D-MESFET based IC's are the most widely used GaAs devices. D-MESFETS have large noise margins, and are the easiest to fabricate, thereby achieving higher yields than other GaAs methods. However, most D-MESFETS require voltage level shifting between drains and gates, as well as two power supplies, restricting density. Random access memories holding 256 bits with 1 ns access times have been made with D-MESFETS.

Enhancement-mode MESFETs use only one power supply and allow denser chips to be fabricated with lower power dissipation. However, E-MESFETs require very thin, lightly doped channel regions that are difficult to fabricate, and have smaller voltage swings which limits their noise immunity. Another drawback is the high resistance of the channel between the gate or drain. Use of the self-aligned gate method employed in NMOS enabled Fujitsu to overcome this problem and fabricate a 1K static RAM.

Other approaches are being developed to realize E-MESFET VLSI circuits, such as recessed gate structures, T-bar gate structures, and JFETs. Finally, the high-electron-mobility transistor (HEMT) is a variation of the E-MESFET which uses a thin electron gas layer to obtain a faster device than possible with conventional MESFETs. But the HEMT is hampered by the lack of production molecular beam epitaxy (MBE) equipment, as well as the usual problems associated with E-MESFETs.

The most sophisticated GaAs device is the heterojunction bipolar transistor (HJBT). It is a vertical device, which uses thin layers of GaAs and AlGaAs, giving it a wide energy bandgap, and constant threshold voltages. This technology promises switching delays on the order of 10 picoseconds. However, it is extremely difficult to fabricate, requiring molecular beam epitaxy (MBE) and ion implantation, and so only circuits of 5 to 10 gates have been demonstrated.

The most significant problem facing gallium arsenide is yield, which is a key factor in determining chip cost. Defect density in the substrate is reported in the range of 10^3 - 10^4 per square centimeter. For chips of 100-gate complexity, yields have been around 25-30%, while for chips of 1,000 gate complexity, yields are below .1%. A major improvement in substrate quality has been achieved, and this should translate into a corresponding increase in yield. A Japanese firm has grown 65mm diameter GaAs crystals with a defect density of less than 200/cm², using the Liquid-Encapsulated Czochralski method.

In the United States, the Defense Advanced Research Projects Agency (DARPA), has been the driving force behind gallium arsenide development.

Under a \$40 million contract with Rockwell International and Honeywell, DARPA is sponsoring a GaAs foundry with the goal of processing 100 3-inch wafers per week by 1986. Besides many high speed logic chips, DARPA is looking to develop two kinds of memories. One is a main memory of 16K capacity (64K if yield permits), with a 10 ns access time and power dissipation of 1 uW/bit. The other is a scratchpad or cache memory holding 1K - 4K, with a 1 ns access time and power dissipation of 100 uW/bit. In addition to the work at Rockwell and Honeywell, DARPA is funding McDonnell Douglas' JFET technology, and Texas Instruments' heterojunction bipolar technology.

While gallium arsenide enjoys a large speed advantage over silicon using the present 1-3 um design rules, this will not always be the case. At the submicron level, the resistance of interconnections and the capacitances between them will become the limiting factors for speed, and the intrinsic speed of the semiconductor material will become secondary. Therefore, gallium arsenide has to reach fruition in the next four to six years, or it will be of little use if at all.

JOSEPHSON TECHNOLOGY

Josephson technology offers extremely fast switching speeds (5 picoseconds), very low power dissipation (.35 uW/gate), superconducting interconnections, and nonvolatile storage. The power-delay product of a Josephson junction ($1.75 \times 10^{-18} \text{J}$) is several orders of magnitude lower than for gallium arsenide. Josephson technology makes use of the fact that certain materials such as lead and niobium become superconductors at extremely low temperatures (below 7° Kelvin). A Josephson junction is made up of two superconductors separated by a thin, insulating layer. A

superconducting current will flow across the insulator as long as the current does not exceed a certain critical value. When this "critical current" is exceeded, the junction takes on a resistance and is no longer superconducting. Two or three Josephson junctions together form an interferometer which is the fundamental switching element in this technology's devices.

A major blow to Josephson junctions was dealt by IBM in September 1983 when it decided to halt further development of a high speed computer based on this technology. The goal of the \$20 million a year research project was a signal processor with a cycle time of around 4 nanoseconds. IBM's work on Josephson technology represented about half of U.S. research in this area. The same year, Sperry Corporation discontinued its work on Josephson junctions, and Bell Labs reduced its program significantly.

The reason for IBM's withdrawal from this technology was difficulty in the development of a cache memory for the computer. The computer's main memory was to be based on a 16K chip with a 15 ns access time, while the cache memory would hold 4K and access in 600 picoseconds. The problem was that the statistical variation in the junction critical current across each chip was too high to allow an acceptable yield of memory chips. The cache memory chip would have to be redesigned to allow for the achieved 1 to 2 percent variation in critical current and yield a satisfactory number of functioning chips. This would have delayed the IBM project's completion until 1988, when advances in silicon and gallium arsenide would make their performance comparable to Josephson technology. By that time, a small increase in performance would not merit a switch to the entirely different Josephson technology.

Despite IBM's retreat from this technology, some work is still being done on Josephson junctions. More importantly, researchers are also searching for superconducting materials which behave more similar to semiconductors than Josephson technology.

NONVOLATILE MEMORIES

Nonvolatile memories are those which do not lose their stored information when power is removed. A simple way to achieve nonvolatility is to use a low power CMOS memory with a battery backup. One drawback to this technique is the additional space needed for the battery. Mostek has overcome this problem with their Zeropower RAM, which is a 16K CMOS static RAM that has two lithium-cell batteries mounted inside its package. However, problems still remain, such as the battery's limited life, questionable reliability, and poor performance at extreme temperatures.

True nonvolatility is offered by the NVRAM or shadow RAM. In the NVRAM, a volatile NMOS static RAM memory cell is merged with the nonvolatile cell found in EEPROMs to form two matched arrays. During normal operation, only the volatile memory array is used. When power is removed, the data is written from the volatile array to the nonvolatile array in a 10 μ s cycle. When power is reapplied, the data is read from the nonvolatile array into the volatile one. Originally, commands were used to perform these operations and a special power supply was needed to give the extra 10 ms of power needed to run the storage cycle. However, the latest devices do the interarray storage and retrieval automatically when power is taken away or reapplied, and no longer require special power sources. The size of the nine-device memory cell required for the NVRAM has limited its capacity to 4K. While 8K NVRAMs are expected in 1985, the

high cost of these devices will hamper further development for larger capacity memories.

MAGNETIC BUBBLE TECHNOLOGY

Bubble memories use two stable states to store data with true nonvolatility. A bubble is a cylindrical magnetic domain which has its polarization opposite in direction to the polarization of the magnetic film in which it is found. The presence of a bubble is interpreted as a "1", while its absence represents a "0". Bubbles are easily generated and annihilated, and can be moved across the film at high velocities. Extremely high density bubble memory chips can be achieved because only one photolithographic layer is required. Four megabit bubble chips are available now, and 16 megabit devices are expected in 1985.

Bubble memories fare well in harsh environments, such as extreme temperatures. Certain bubble memory subsystems are able to function from -20°C to $+85^{\circ}\text{C}$, and soon will have a functional temperature range of -55°C to $+85^{\circ}\text{C}$. Bubble memories also can withstand such extremes as dust, shock, and vibration.

The major drawback to this technology is due to the fact that the bubble chip is essentially a serial access device. Magnetic bubbles are circulated in a major and many minor loops, and several support chips are needed to achieve random access capability. This fact is responsible for the bubble memory's slow access time, which is on the order of 40 milliseconds for most devices. Also, the bubble memory subsystem consumes a lot of power. While one megabit of silicon RAM consumes about .5 watts, a megabit bubble chip and its five support chips will typically use 1.7 watts. For this reason, bubble memories are not a threat to replace

semiconductor main memories, but are seen rather as a rugged replacement for mass storage disk drives.

MAGNETIC CROSSTIE MEMORIES

Another, newer magnetic storage device is the crosstie random access memory (CRAM). Binary information is represented by the presence or absence of a crosstie-Block line pair on a Néel wall. The crosstie is a stable magnetic state constituting a transition between Block walls of thick film and Néel walls of very thin films. Like magnetic bubble memory, the CRAM is nonvolatile, has a wide temperature range (-190°C to $+196^{\circ}\text{C}$) and is radiation hard, able to withstand a 1 megarad dose without upset. However, unlike bubble memory, the CRAM offers true random access, and access times comparable to semiconductor memories have been achieved. All the necessary support circuitry can be built right onto the CRAM chip, because the magnetic Permalloy film is deposited upon silicon.

Magnetic crosstie technology has been around for more than 20 years, but has only recently been applied to random access memories. Consequently, only 256-bit test devices have been produced, with 1K, 30 nanosecond CRAMs expected in 1985. The Navy is developing crosstie memories as a replacement for magnetic core and plated wire memories, with the goal of 16K, 70 nanosecond devices within five years. The only drawback to this technology is that the CRAM has a higher active power dissipation than nonvolatile semiconductor memories.

CONCLUSION

Bulk CMOS can be expected to dominate main memory applications until silicon-on-insulator comes of age in the 1990's. The realization of three dimensional circuits will determine the eventual success of SOI. Gallium arsenide will have to overcome its problems by 1990 if it is to replace silicon for cache, scratchpad and buffer applications. Beyond that point, the submicron geometries will reduce the benefits of a faster substrate. Whatever substrate is used, the interconnection problems must be solved in order to realize .5 um devices.

Nonvolatile memory technology presently offers the choice of semiconductor NVRAMs with high speeds and low capacity and bubble memories with low speeds and high capacity. The magnetic crosstie memory holds the potential for bridging the gap, promising high capacity devices and semiconductor-like speeds, along with a wide temperature range and radiation hardness.

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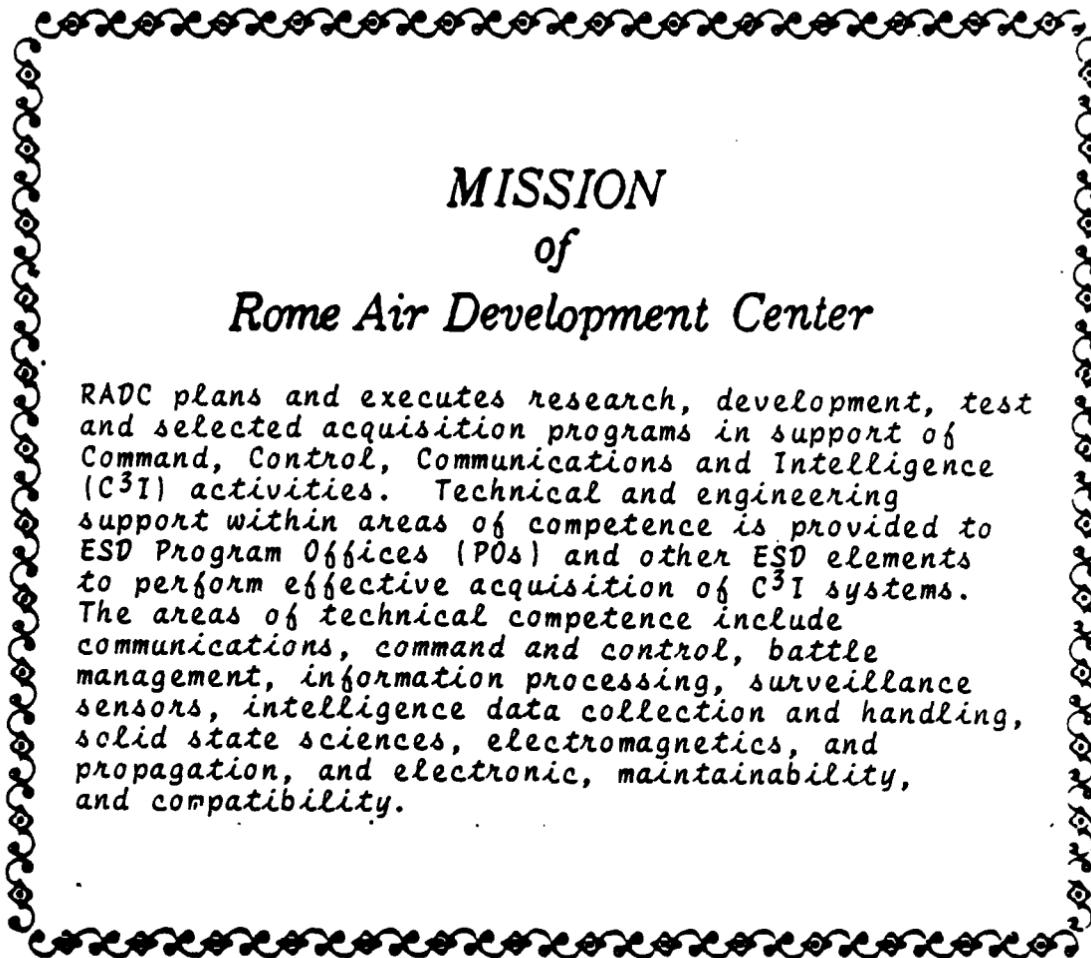
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